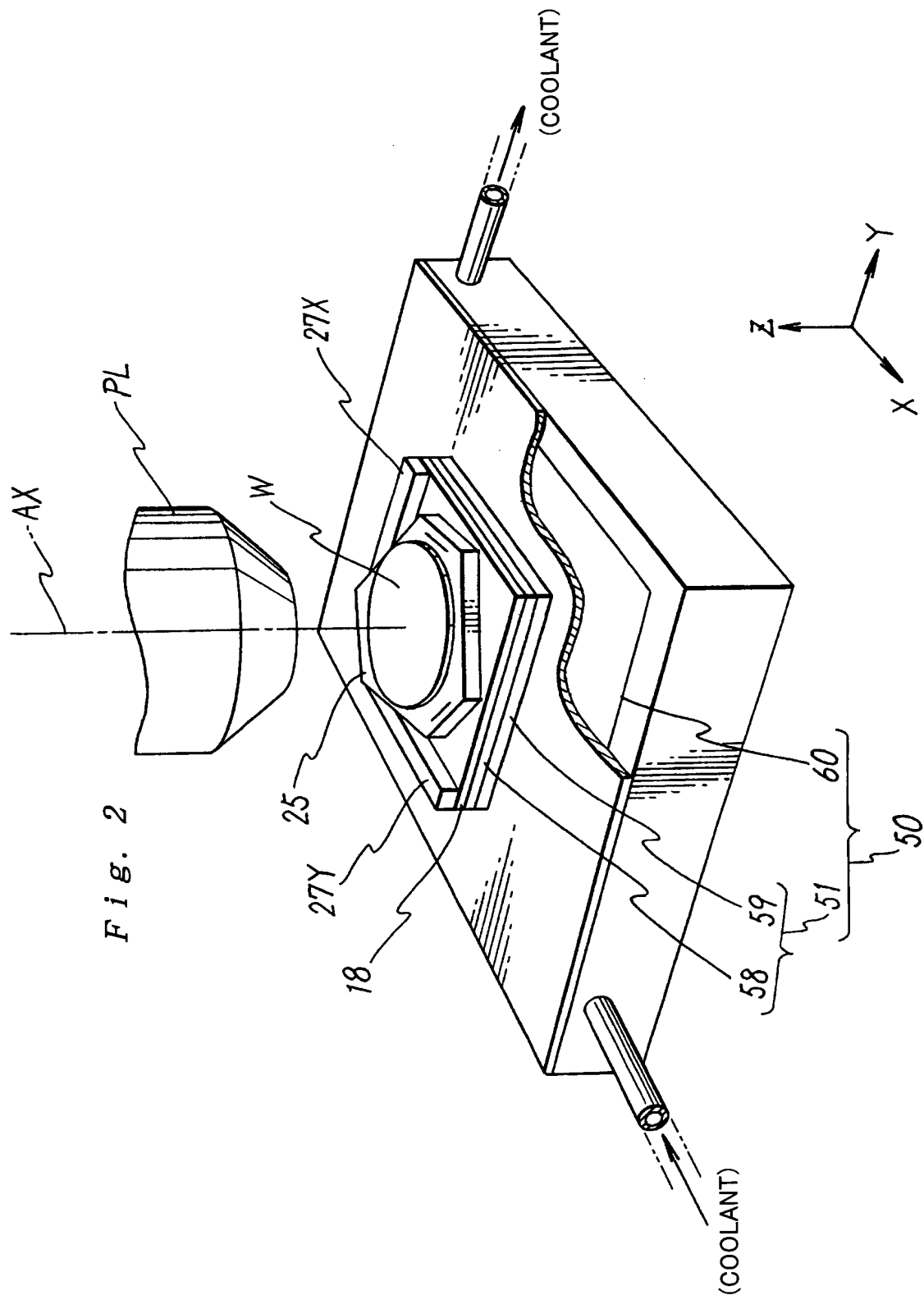
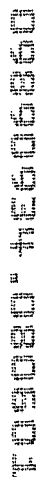


The schematic diagram illustrates a semiconductor device manufacturing apparatus 100. It includes a main controller 20 connected to several processing units. A substrate 7 is positioned on a stage 15, which is part of a larger assembly 16. The substrate 7 has a surface 10. A coordinate system is shown at the bottom right, with Z pointing up, X pointing left, and Y pointing right. Various other components are labeled, including 19, 80, 22, SC, SID, ID, 79, 21, 50, 51, 60, 18, 27, 31, 30, W, PL, AX, RST, R, IX, IL, and 10.

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Top view of the device. A series of seven rectangular elements are arranged horizontally. From left to right, they are labeled 53N, 54S, 54N, 54S, 54N, 54S, and 53N. A coordinate system is shown with X, Y, and Z axes.

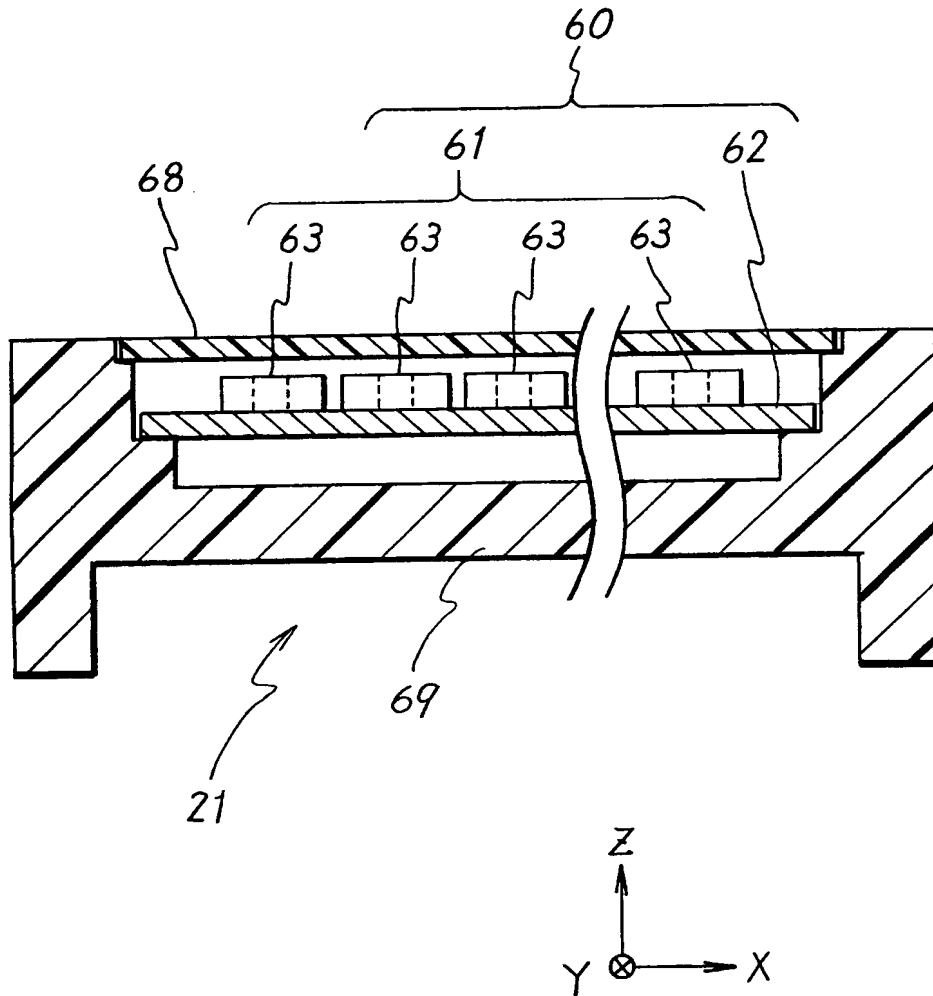
54S 52N 52S 52N 52S 52N 54S

59

Y X Z

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Fig. 4



09890934 08660

Fig. 5A

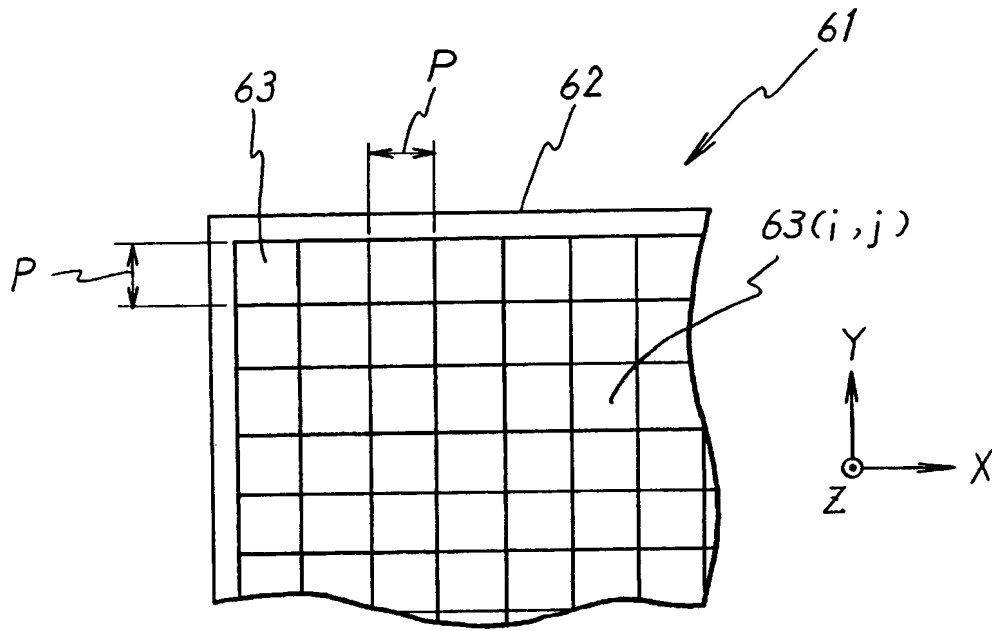


Fig. 5B

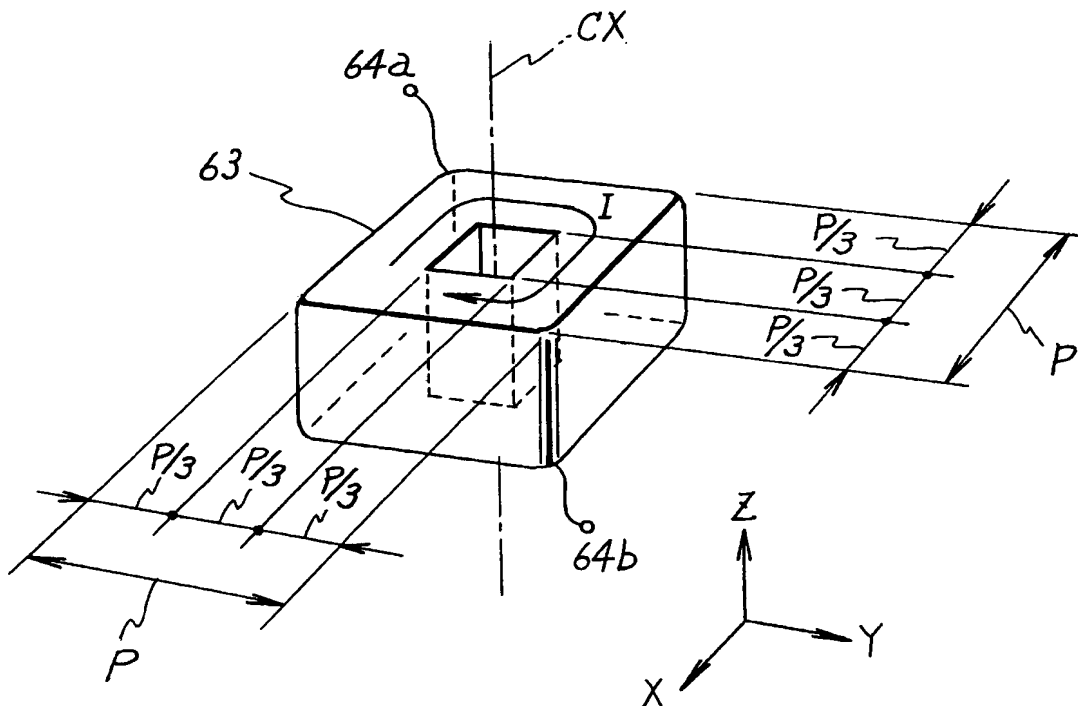


Fig. 6

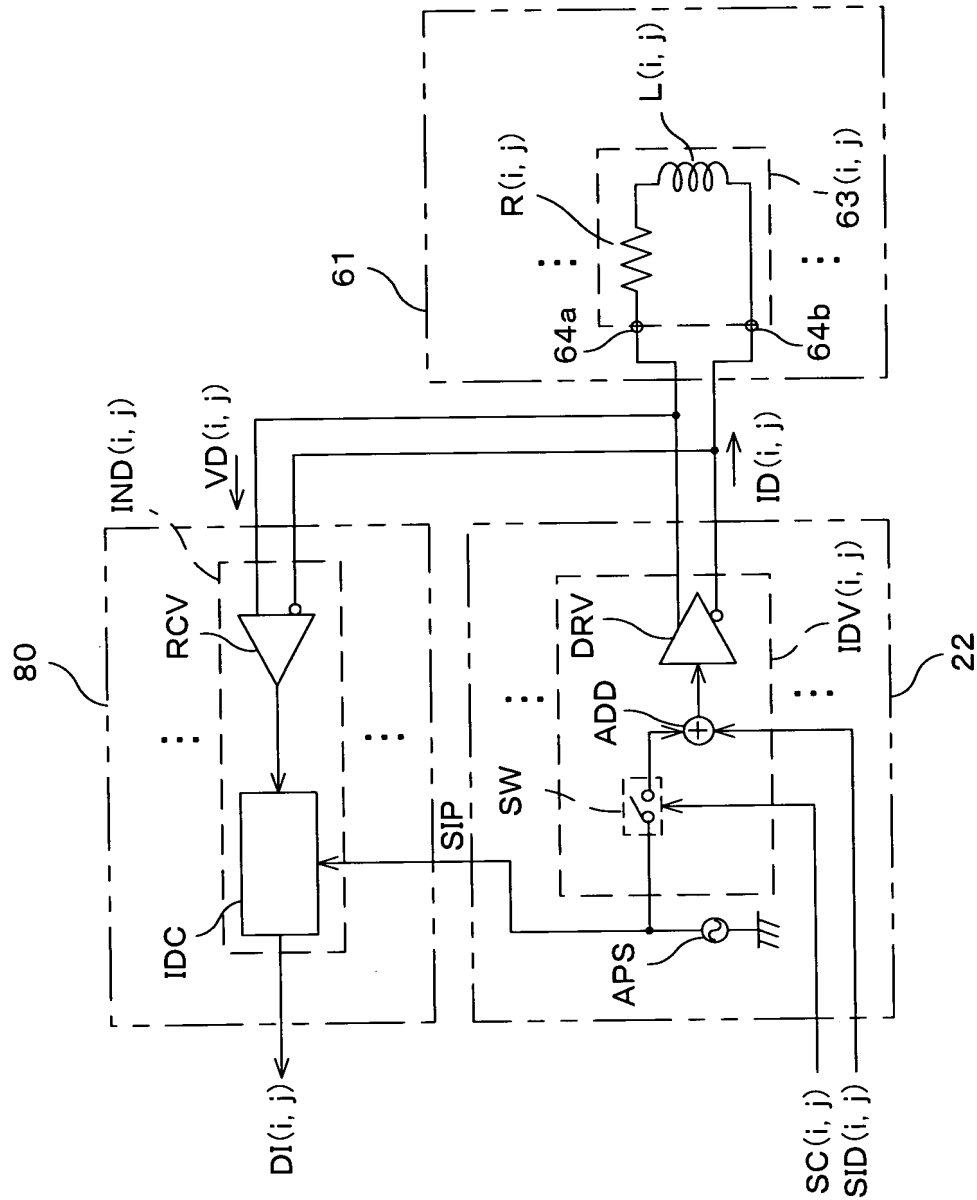


Fig. 7A

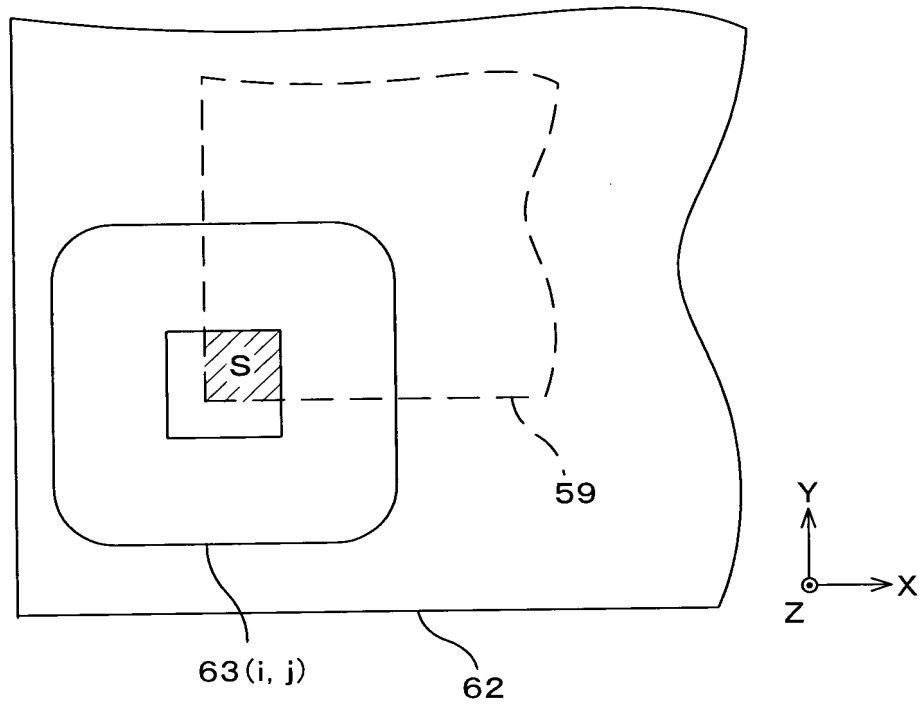


Fig. 7B

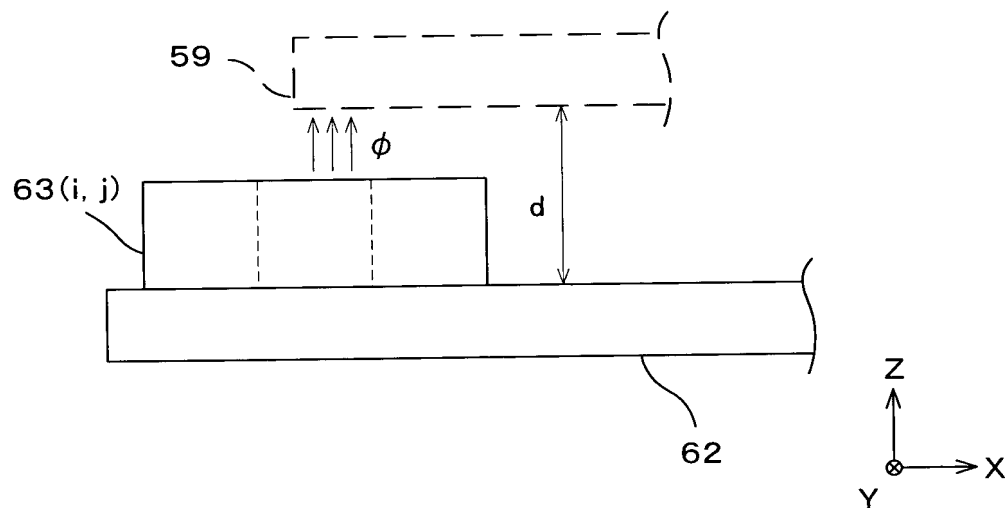


Fig. 8A

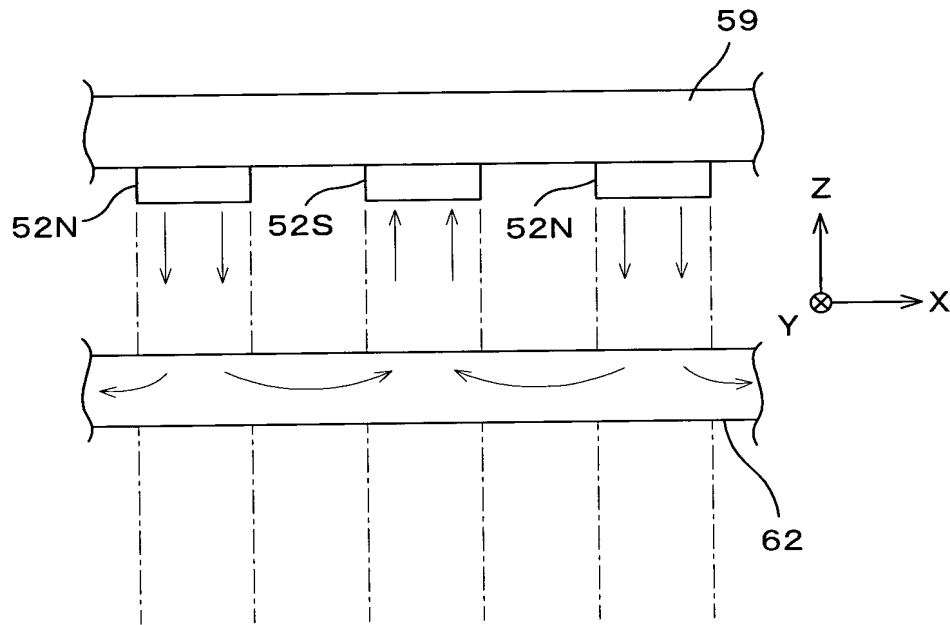


Fig. 8B



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Fig. 9A

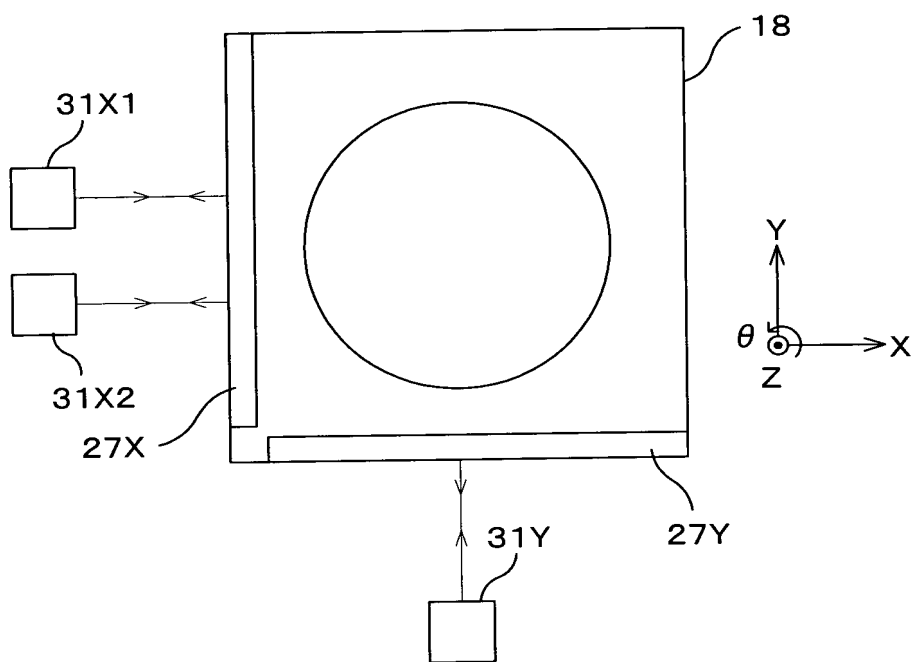
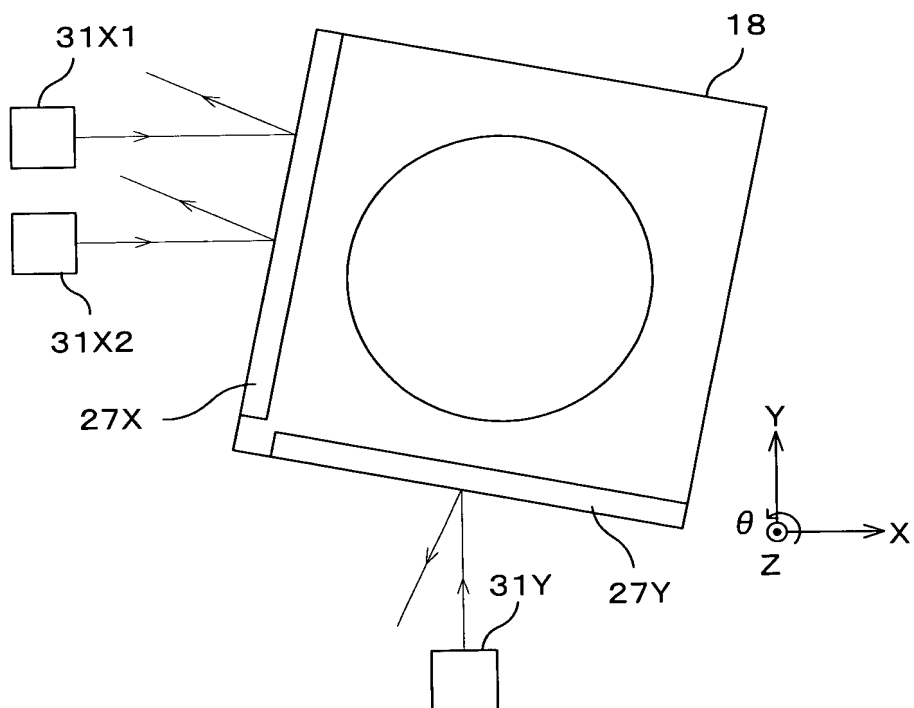


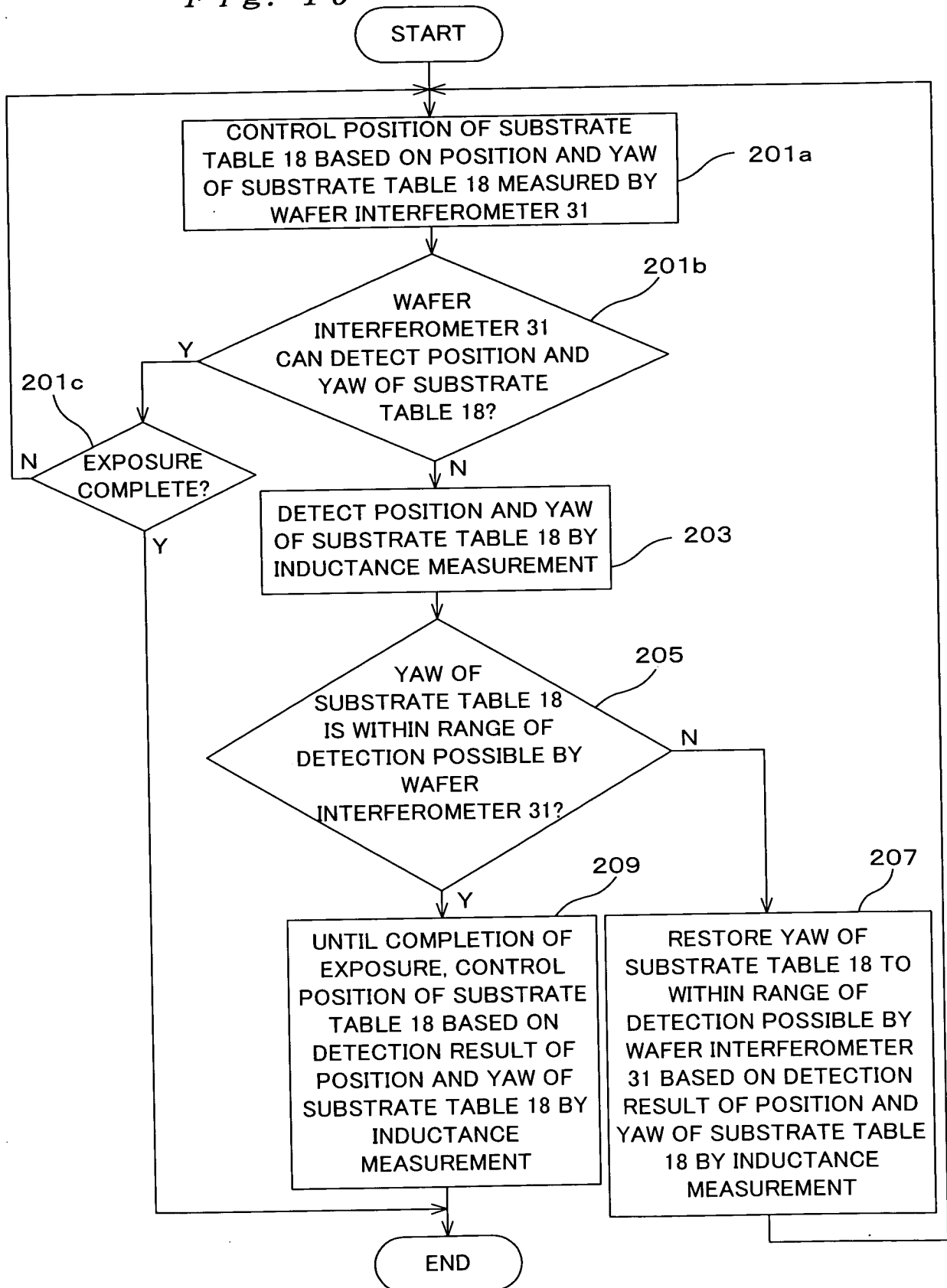
Fig. 9B



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Fig. 10



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Fig. 11

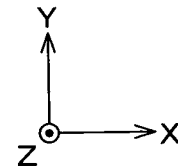
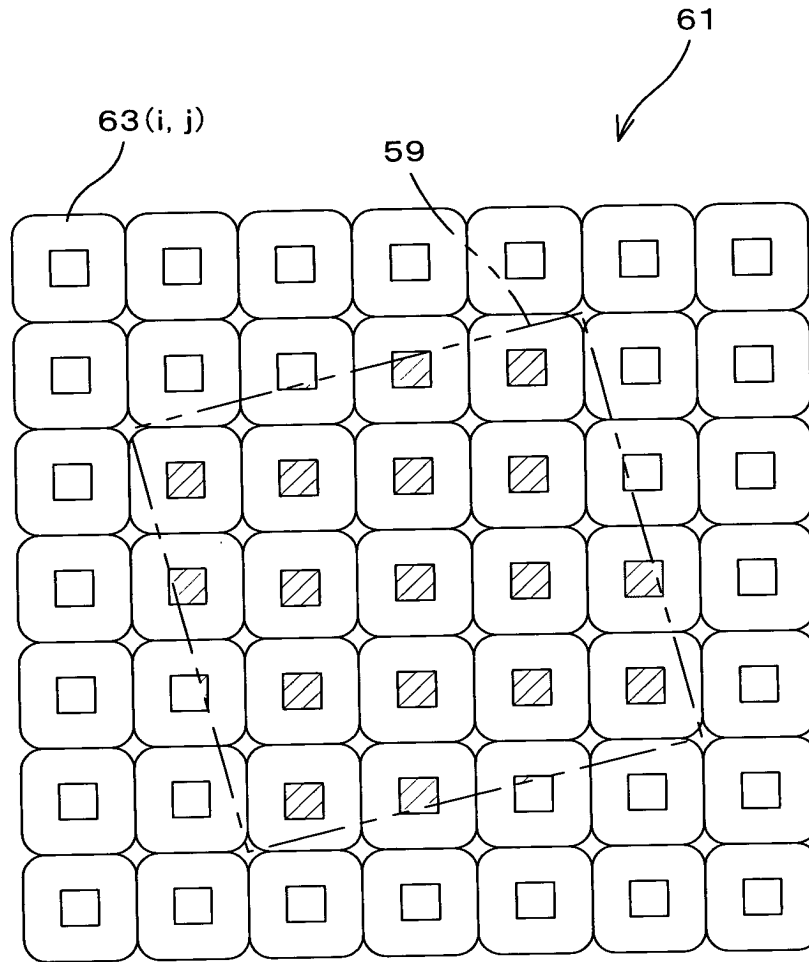
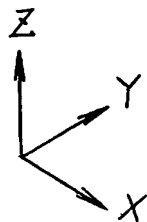


Fig. 12

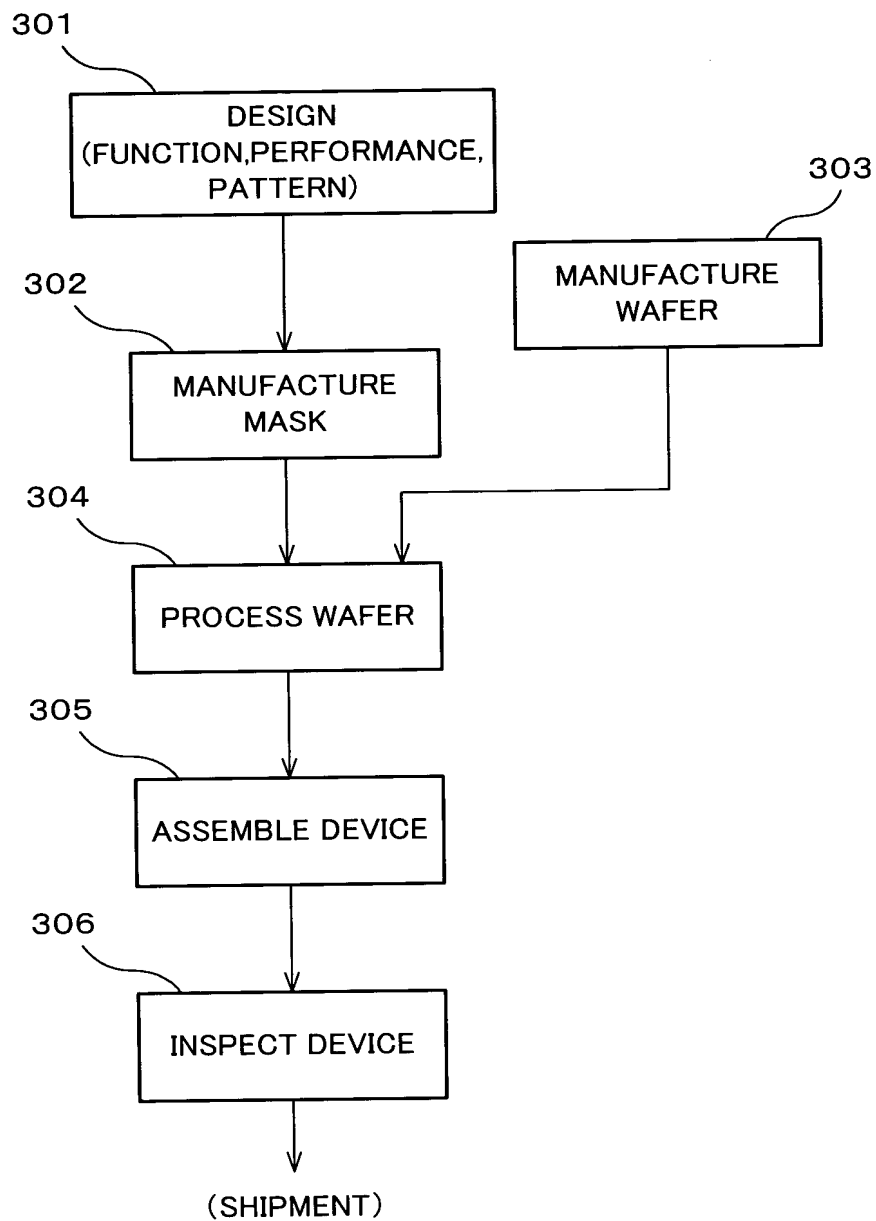
61

63(i, j)

L=0	L=0	L=0	L=0	L=0	L=0	L=0
L=0	L=0	L=0.1	L=0.9	L=1	L=0	L=0
L=0	L=1	L=1	L=1	L=1	L=0.1	L=0
L=0	L=0.9	L=1	L=1	L=1	L=0.9	L=0
L=0	L=0.1	L=1	L=1	L=1	L=0.1	L=0
L=0	L=0	L=1	L=0.9	L=0.1	L=0	L=0
L=0	L=0	L=0	L=0	L=0	L=0	L=0

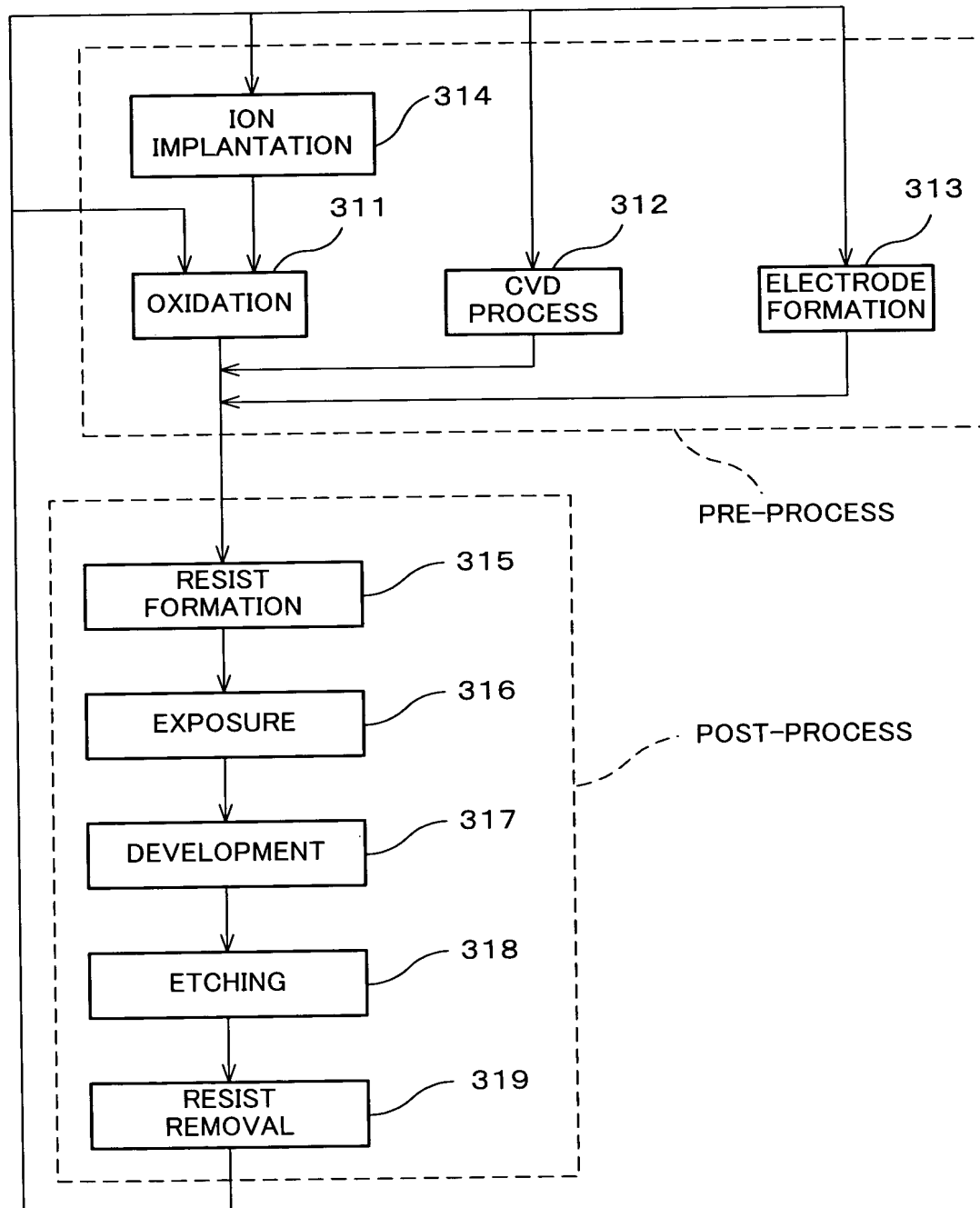


F i g. 14

[illegible]

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Fig. 15



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Fig. 16A

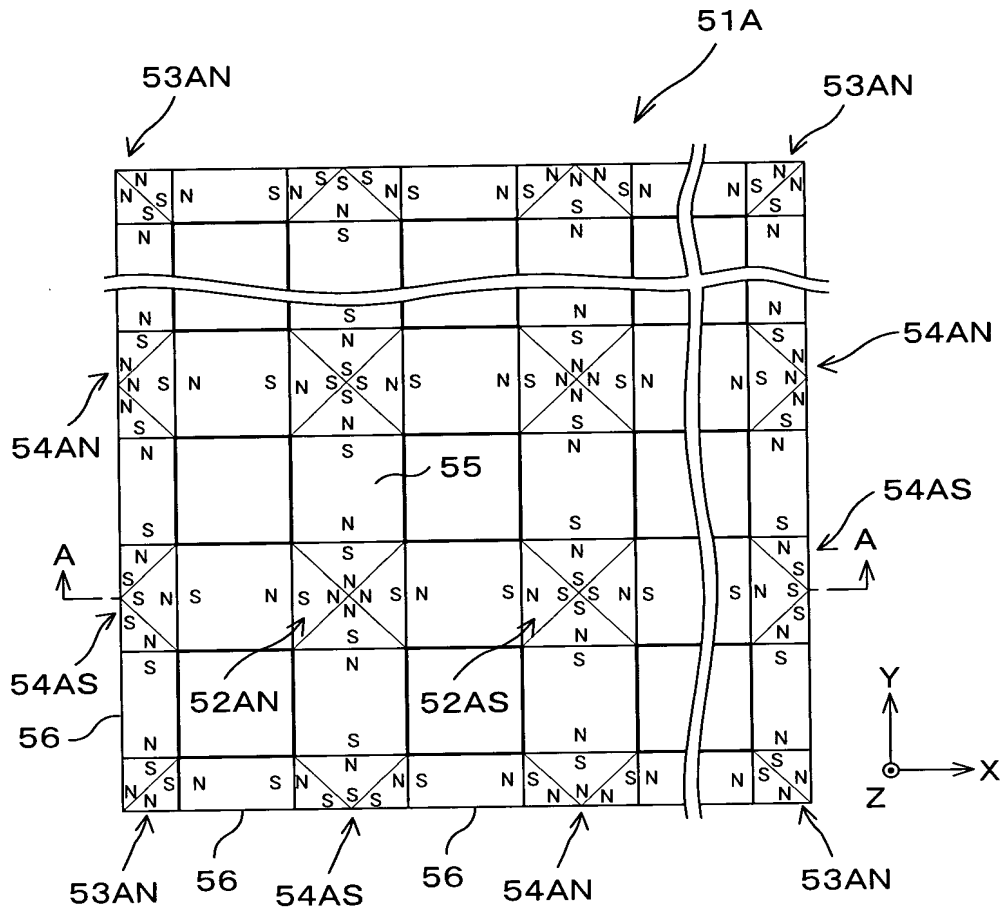


Fig. 16B

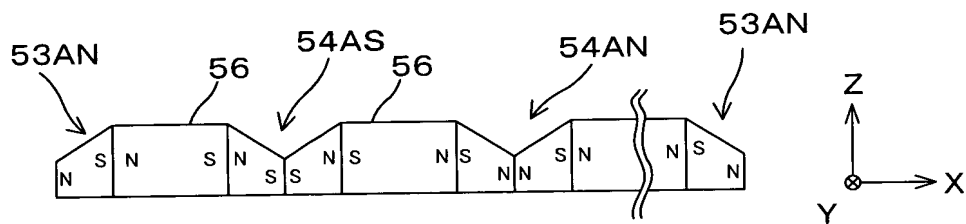
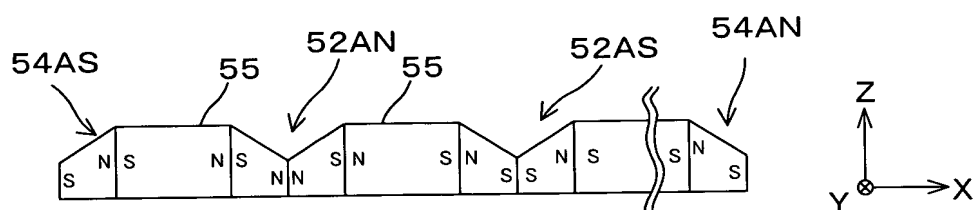


Fig. 16C



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Fig. 17

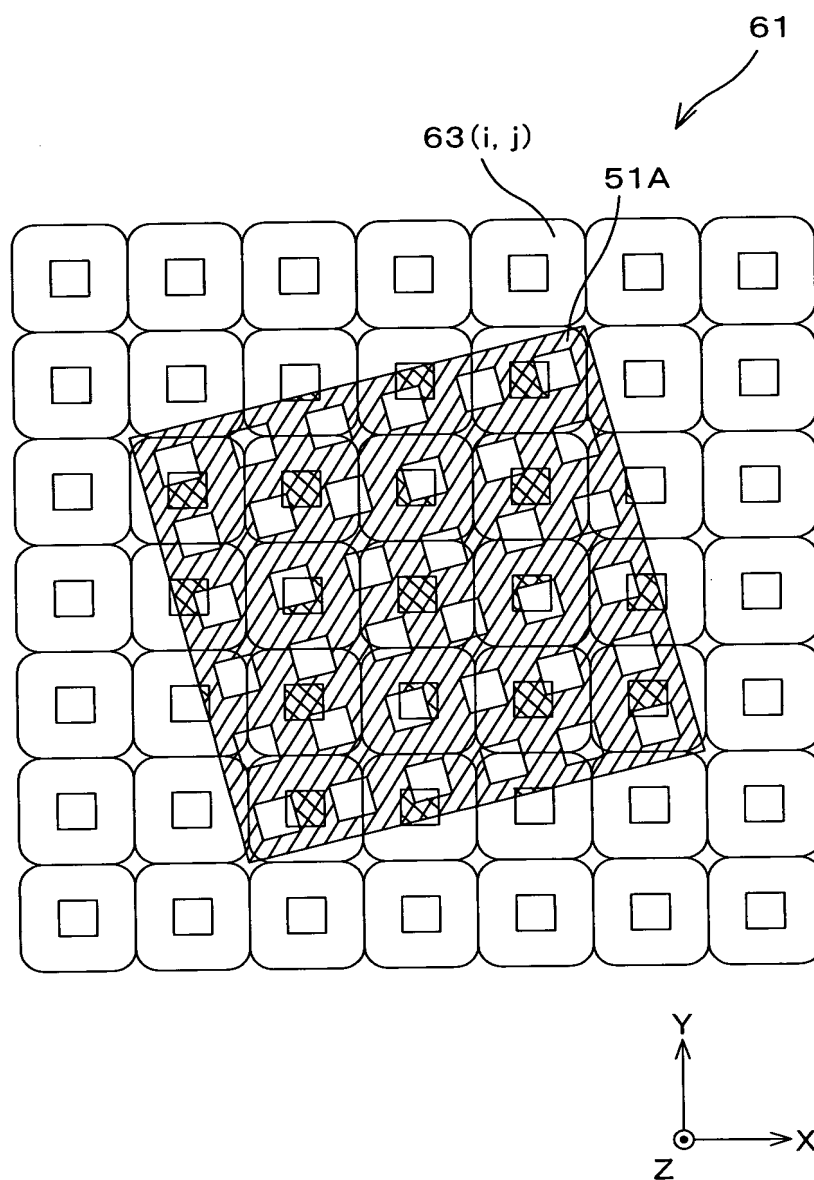


Fig. 18A

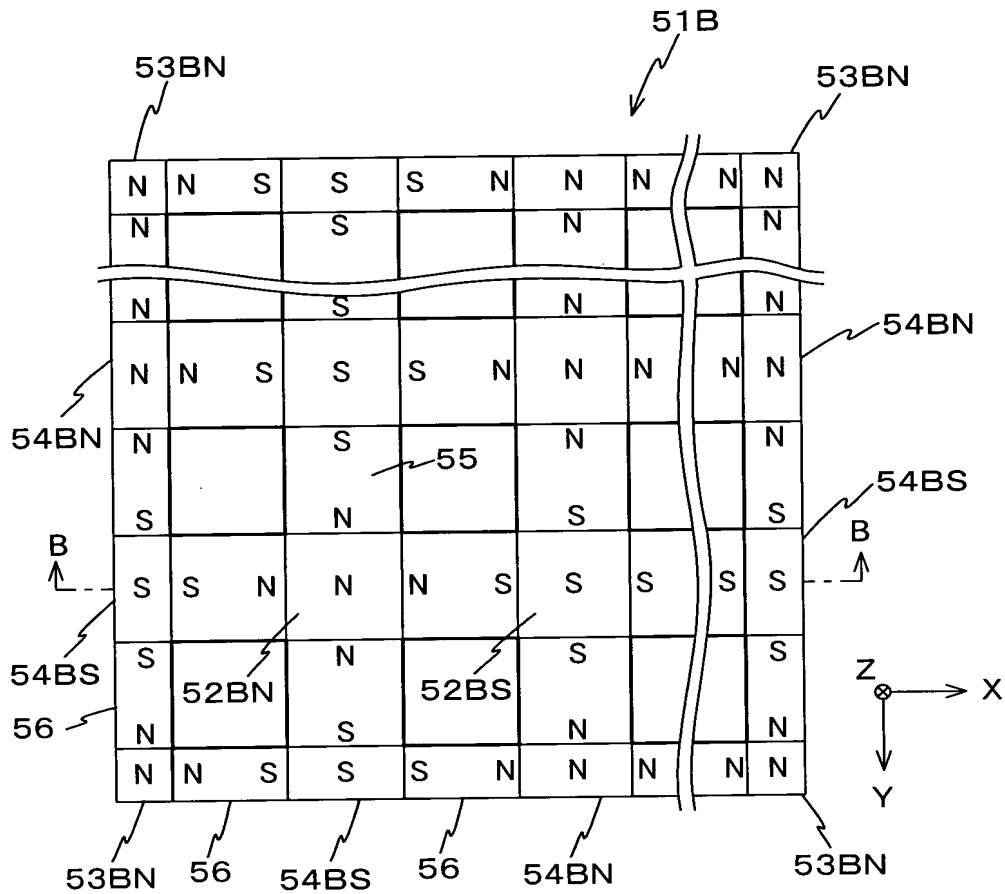


Fig. 18B

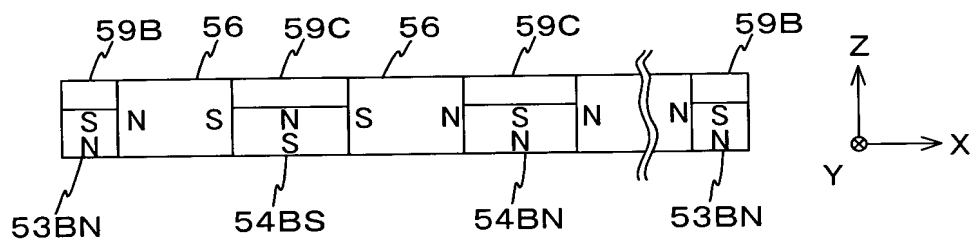


Fig. 18C

